REMARKS

This paper is responsive to the Non-Final Office Action dated March 8, 2005. Claims 1-42 were examined. Claims 1-10, 12-13, and 15-42 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Publication No. 2004/0223393 to Hush et al. Claims 11, 14 are objected to as being dependent upon a rejected base claim.

Drawings

Figures 2, 3, 6 and 7 are amended to clarify circuit connection points.

Specification

The specification is amended to include updated patent application information.

Claim Rejections Under 35 U.S.C. § 102(e)

Claims 1-10, 12-13, and 15-42 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Publication No. 2004/0223393 to Hush et al. Regarding claim 1, Applicants respectfully maintain that Hush, alone or in combination with other references of record, fails to teach or suggest

> a test block configured to characterize in situ a sensing offset of a sensing circuit including a cross-coupled pair of transistors,

as required by claim 1. The Office Action relies on the Abstract and claim 7 of Hush to supply this teaching. These portions of Hush teach that

> [a] variable resistance memory sense amplifier has a built-in offset to assist in switching the sense amplifier when a resistive memory cell is in a low resistance state. The built-in offset can be achieved by varying size, threshold voltage, associated capacity or associated resistance of the transistors within the sense amplifier.

(Abstract, emphasis added) The offset of the memory sense amplifier is intentionally unbalanced by fabrication techniques. [0005, 0020] Nowhere does Hush teach or suggest characterizing the offset of the cross-coupled pair of transistors in the memory sense amplifier of Hush. Instead,

Hush teaches using the memory sense amplifier to detect two voltage states of the resistive memory cell in the presence of a defective reference memory cell. [0002, 0018] These two voltage states of the resistive memory cell of Hush are not sensing offsets, as claimed. In addition, Hush fails to teach or suggest that the resistive memory cells include a cross-coupled pair of transistors, as claimed. For at least these reasons, Applicants respectfully maintain that claim 1 distinguishes over Hush and all references of record. Accordingly, Applicants respectfully request that the rejection of claim 1 and all claims dependent thereon, be withdrawn.

Regarding claim 5, Applicants respectfully maintain that Hush, alone or in combination with other references of record, fails to teach or suggest that

> the sensing offset results, at least in part, from an accumulated data-dependent mismatch in characteristics of the cross-coupled transistors,

as required by claim 5. As described above, the offset of the memory sense amplifier of Hush is intentionally unbalanced by fabrication techniques. [0005, 0020] Nowhere does Hush, alone or in combination with other references of record teach or suggest that the offset of the memory sense amplifier results from an accumulated data-dependent mismatch in characteristics of the cross-coupled transistors, as claimed and described in the specification at least in paragraph 1019. For at least this reason, Applicants respectfully maintain that claim 5 distinguishes over Hush and all references of record. Accordingly, Applicants respectfully request that the rejection of claim 5 and all claims dependent thereon, be withdrawn.

Claim 8 is amended to clarify the invention. Regarding amended claim 8, Applicants respectfully maintain that Hush, alone or in combination with other references of record, fails to teach or suggest

> at least a first and a second discharge path coupled to at least one of the respective first and second plurality of ports, the effective strengths of the first and second discharge paths determined by respective ones of the first and second plurality of

> control signals, the first and second discharge paths configurable for characterization of a sensing offset associated with a sensing circuit,

as required by amended claim 8. Hush teaches that

> [a] variable resistance memory sense amplifier has a built-in offset to assist in switching the sense amplifier when a resistive memory cell is in a low resistance state. The built-in offset can be achieved by varying size, threshold voltage, associated capacity or associated resistance of the transistors within the sense amplifier.

(Abstract, emphasis added) The offset of the memory sense amplifier is intentionally unbalanced by fabrication techniques. [0005, 0020] Nowhere does Hush teach or suggest characterizing the offset of the cross-coupled pair of transistors in the memory sense amplifier of Hush. Instead, Hush teaches using the memory sense amplifier to detect two voltage states of the resistive memory cell in the presence of a defective reference memory cell. [0002, 0018] These two voltage states of the resistive memory cell of Hush are not sensing offsets, as claimed. For at least this reason, Applicants respectfully maintain that claim 8 distinguishes over Hush and all references of record. Accordingly, Applicants respectfully request that the rejection of claim 8 and all claims dependent thereon, be withdrawn.

Regarding claim 17, Applicants respectfully maintain that Hush, alone or in combination with other references of record, fails to teach or suggest

> additional control signals at least partially compensating for the detected sensing offset by selectively exposing one of the transistors of a sensing circuit to a bias voltage selected to cause a compensating shift in a characteristic of the exposed transistor,

as recited by claim 17. As described above, the offset of the memory sense amplifier of Hush is intentionally unbalanced by fabrication techniques. [0005, 0020] Nowhere does Hush, alone or in combination with other references of record teach or suggest exposing one of the transistors of

a sensing circuit to a bias voltage selected to cause a shift in a characteristic of the exposed transistor to compensate for a detected sensing offset of a sensing circuit. For at least this reason, Applicants respectfully maintain that claim 17 distinguishes over Hush and all references of record. Accordingly, Applicants respectfully request that the rejection of claim 17 and all claims dependent thereon, be withdrawn.

Regarding claim 26, Applicants respectfully maintain that Hush, alone or in combination with other references of record, fails to teach or suggest

> detecting in situ a sensing offset in a sensing circuit including a pair of cross-coupled transistors,

as recited by claim 26. The Office Action apparently relies on the Abstract and claim 7 of Hush to supply this teaching. These portions of Hush teach that

> [a] variable resistance memory sense amplifier has a built-in offset to assist in switching the sense amplifier when a resistive memory cell is in a low resistance state. The built-in offset can be achieved by varying size, threshold voltage, associated capacity or associated resistance of the transistors within the sense amplifier.

(Abstract, emphasis added) The offset of the memory sense amplifier is intentionally unbalanced by fabrication techniques. [0005, 0020] Nowhere does Hush teach or suggest characterizing the offset of the cross-coupled pair of transistors in the memory sense amplifier of Hush. Instead, Hush teaches using the memory sense amplifier to detect two voltage states of the resistive memory cell in the presence of a defective reference memory cell. [0002, 0018] These two voltage states of the resistive memory cell of Hush are not sensing offsets, as recited by claim 26. For at least this reason, Applicants respectfully maintain that claim 26 distinguishes over Hush and all references of record. Accordingly, Applicants respectfully request that the rejection of claim 26 and all claims dependent thereon, be withdrawn.

Regarding claim 41, Applicants respectfully maintain that Hush, alone or in combination with other references of record, fails to teach or suggest

> means for detecting in situ a sensing offset in a sensing circuit that includes a cross-coupled pair of transistors

as recited by claim 41. The Office Action apparently relies on the Abstract and claim 7 of Hush to supply this teaching. These portions of Hush teach that

> [a] variable resistance memory sense amplifier has a built-in offset to assist in switching the sense amplifier when a resistive memory cell is in a low resistance state. The built-in offset can be achieved by varying size, threshold voltage, associated capacity or associated resistance of the transistors within the sense amplifier.

(Abstract, emphasis added) The offset of the memory sense amplifier is intentionally unbalanced by fabrication techniques. [0005, 0020] Nowhere does Hush teach or suggest characterizing the offset of the cross-coupled pair of transistors in the memory sense amplifier of Hush. Instead, Hush teaches using the memory sense amplifier to detect two voltage states of the resistive memory cell in the presence of a defective reference memory cell. [0002, 0018] These two voltage states of the resistive memory cell of Hush are not sensing offsets, as claimed. In addition, Hush fails to teach or suggest that the resistive memory cells include a cross-coupled pair of transistors, as claimed. For at least these reasons, Applicants respectfully maintain that claim 41 distinguishes over Hush and all references of record. Accordingly, Applicants respectfully request that the rejection of claim 41 and all claims dependent thereon, be withdrawn.

Allowable Subject Matter

Applicants appreciate the indication of allowable subject matter in claims 11 and 14. Applicants believe that claims 11 and 14 depend from allowable base claims and are allowable for at least this reason.

Claim 23 is cancelled. Claim 16 is amended consistent with amendments to claim 8.

In summary, claims 1-22 and 24-42 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited.

Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

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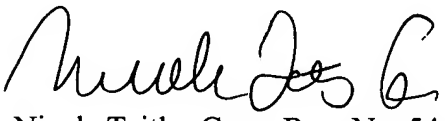
Respectfully submitted,



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AMENDMENTS TO THE DRAWINGS

The attached sheet(s) of drawings include changes to Fig(s). 2, 3, 6, and 7 and replace the original sheet(s) including such figures.

Attachment(s): Replacement Sheet including amended Fig. 2;
Replacement Sheet including amended Fig. 3;
Replacement Sheet including amended Fig. 6 and amended Fig. 7;
Annotated Sheet Showing Changes to amended Fig. 2;
Annotated Sheet Showing Changes to amended Fig. 3; and
Annotated Sheet Showing Changes to amended Fig. 6 and amended Fig. 7.